IN THE CLAIMS:

Listing of claims:

1. (currently amended) A method for manufacturing a semiconductor device, the method comprising:

(a) forming a gate dielectric layer over a semiconductor substrate;

(b) forming a gate electrode over the gate dielectric layer;

(c) forming a dielectric layer over the semiconductor substrate;

(d) forming a mask layer over the dielectric layer;

(e) anisotropically etching the mask layer to form a sidewall mask layer on sides of the gate electrode over the dielectric layer;

(f) isotropically etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer; and

(g) ~~forming a first impurity layer and a second impurity layer by~~ ion-implanting an impurity in the semiconductor substrate, wherein the ion-implanting includes implanting an impurity through the extension control layer into the semiconductor substrate and the implanting also includes implanting an impurity directly into the semiconductor substrate in a region adjacent to the extension control layer; ~~and~~

wherein an extension region is formed in the semiconductor substrate below the extension control layer during the ion-implanting, and source and drain regions are formed in the semiconductor substrate adjacent to the extension region; and ~~used to form the first impurity layer and the second impurity layer~~

(h) forming a metal layer over the semiconductor substrate and heating the metal layer to form a silicide on upper portions of the source and drain regions and on an upper portion of the gate electrode; wherein the extension control layer above the extension region inhibits the formation of a silicide on the extension control layer during the heating.

2. (previously presented) A method for manufacturing a semiconductor device according to claim 1, wherein the step (f) further includes the step of forming a sidewall protection layer on sidewalls of the gate electrode.

3. (currently amended) A method for manufacturing a semiconductor device according to claim 2, further including removing the sidewall mask layer after the isotropically etching the dielectric layer and prior to the ion-implanting. ~~forming a first impurity layer and a second impurity layer.~~

4. (original) A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon nitride.

5. (original) A method for manufacturing a semiconductor device according to claim 4, wherein the sidewall mask layer is formed from a material comprising silicon oxide.

6. (original) A method for manufacturing a semiconductor device according to claim 3, wherein the extension control layer is formed from a material comprising silicon oxide.

7. (original) A method for manufacturing a semiconductor device according to claim 6, wherein the sidewall mask layer is formed from a material comprising silicon nitride.

8. (original) A method for manufacturing a semiconductor device according to claim 1, wherein the extension control layer has a thickness of 5 – 50 nm.

9. (original) A method for manufacturing a semiconductor device according to claim 3, wherein the sidewall mask layer is formed to a thickness of 30 – 200 nm.

10-20. (canceled)

21. (currently amended) A method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer by forming a dielectric layer on the semiconductor substrate, forming a mask layer on the dielectric layer, anisotropically etching the mask layer to form a sidewall mask layer, and isotropically etching the dielectric layer after forming the sidewall mask layer; and

~~an~~ a single ion-implanting ~~step~~ operation that forms extension regions in the semiconductor substrate under the extension control structures and forms source and drain ~~source/drain~~ regions in the semiconductor substrate adjacent to the extension regions, ~~layer,~~ wherein the extension regions have a depth that is less than that of the source/drain regions, and wherein the ion-implanting operation includes implanting through the extension control structures to form the extension regions, and the ion-implanting operation includes implanting directly into the semiconductor substrate adjacent to the extension control structures to form the source and drain regions at the same time that the extension regions are being formed.

22. (previously presented) A method according to claim 21, further comprising forming sidewall protection structures on sidewalls of the gate electrode during the isotropically etching the dielectric layer.

23. (previously presented) A method according to claim 22, further comprising removing the sidewall mask layer prior to the ion-implanting.

24. (previously presented) A method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from silicon nitride and the sidewall mask is formed from silicon oxide.

25. (currently amended) A method according to claim 21, wherein the extension control layer is formed from silicon oxide ~~ion-implanting step is carried out as a single ion-implantation operation~~.

26. (previously presented) A method according to claim 22, wherein the extension control layer and the sidewall protection layer are formed from silicon nitride and the sidewall mask layer is formed from silicon oxide.

27. (new) A method according to claim 1, wherein the ion-implanting is carried out in a single ion implanting operation.

28. (new) A method for manufacturing a semiconductor device, comprising:

forming a gate dielectric layer on a semiconductor substrate;

forming a gate electrode on the gate dielectric layer;

forming a dielectric layer on the semiconductor substrate;

forming a mask layer on the dielectric layer;

etching the mask layer to form a sidewall mask layer on sides of the gate electrode;

etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer; and

forming an extension region in the semiconductor substrate by ion-implanting impurity ions into the substrate through the extension control layer;

forming source and drain regions in the semiconductor substrate by ion-implanting impurity ions into the substrate;

forming a metal layer on the gate electrode and the source and drain regions; and

heating the metal to form a silicide on the gate electrode and on the source and drain regions, wherein silicide is inhibited from forming on the extension control layer by the extension control layer.

29. (new) A method as in claim 28, further comprising forming the extension region and the source and drain regions during the same ion-implanting operation.